Amendments To the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A switch coupled between a plurality of host units and a device for routing frame information therebetween and comprising:

a. a first serial advanced technology attachment (ATA) port including a first host task file responsive to a non-data frame information structure (FIS) from a first host unit;

b. a second serial ATA port including a second host task file, responsive to a non-data FIS from a second host unit;

c. a third serial ATA port[,] including a device task file responsive to a non-data FIS from a device, the device configured to support command queuing and operative to generate an original queue depth value indicative of the number of commands that the device can queue from either of the first or second host units; and

d. an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state and whenever either one of the first or second host units sends non-data FIS to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin [and/or] or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive, the arbitration and control circuit being responsive to the original queue depth value and operative to alter the original queue depth value to be a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value

to the first and second host units to be less than that which it is thereby preventing commands being lost by an overrun of the original queue depth value by either of the first or second host units.

Claim 2 (original): A switch as recited in claim 1 wherein said device is a storage unit.

Claim 3 (original): A switch as recited in claim 1 wherein said switch is employed in an enterprise system.

Claim 4 (original): A switch as recited in claim 1 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 5 (previously presented): A switch as recited in claim 1 wherein a bit is used to indicate which host is the origin or destination of the non-data FIS.

Claim 6 (currently amended): A switch as recited in claim 1 wherein said first, second and third SATA ports are layer 2 ports.

Claim 7 (original): A switch as recited in claim 1 wherein the switch provides for 'route aware' routing.

Claim 8 (previously presented): A switch as recited in claim 1 wherein the switch further includes a dual ported first-in-first-out (FIFO).

Claim 9 (currently amended): A switch comprising:

a. a first serial advanced technology attachment [(ATA)] SATA port including a first host task file for connection to a first host unit, said first [ATA] SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second [serial ATA] SATA port including a second host task file for connection to a second host unit responsive to a non-data FIS from the second host unit;

c. a third [serial ATA] SATA port[,] including a device task file responsive to a non-data FIS, for connection to a device, the switch for routing frame information between the first and second host units and the device, the device operative to support command queuing and having an original queue depth value indicative of the number of commands that the device can queue from either of the first or second host units; and

d. an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either one of the first or second host units sends non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin [and/or] or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive, further wherein the arbitration and control circuit is responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less that that which it is so as to avoid commands being lost by overrun of the original queue depth value by either of the first or second host units..

Claim 10 (previously presented): A switch as recited in claim 9 wherein the switch provides for 'route aware' routing.

Claim 11 (original): A switch as recited in claim 9 wherein said device is a storage unit.

Claim 12 (original): A switch as recited in claim 9 wherein said switch is employed in an enterprise system.

Claim 13 (original): A switch as recited in claim 9 wherein said arbitration and control causes concurrent access of the device by the first and second host units.

Claim 14 (currently amended): A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, for routing frame information between the first and second host units and the device, said switch comprising:

a. a first serial ATA port, including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second serial ATA port, including a second host task file for connection to a second host unit, responsive to a non-data FIS from the second host unit;

c. a third serial ATA port[,] including a device task file responsive to a non-data FIS, for connection to a device, the device operative to support command queuing and having an original queue depth value indicative of the number of commands that the device can queue from either of the first or second host units;

d. an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting one of the first or second host units to concurrently access the device through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either the first or second host units sends non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, the other one of to the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin [and/or] or destination host so that routing of non-data FIS is transparent to the switch thereby

reducing the complexity of the design of the switch rendering its manufacturing less expensive,

further wherein, the arbitration and control circuit responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned a number of commands that is less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less that that which it is thereby preventing commands being lost by an overrun of the original queue depth value by either of the first or second host units.

Claim 15 (original): A switch as recited in claim 14 wherein the switch is a serial ATA switch.

Claim 16 (original): A switch as recited in claim 14 wherein said device is a storage unit.

Claim 17 (original): A switch as recited in claim 14 wherein said switch is employed in an enterprise system.

Claim 18 (original): A switch as recited in claim 14 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 19 (currently amended): A method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween comprising:

a. receiving a non-data frame information structure (FIS) through a first serial ATA port, from a first host unit;

b. receiving a non-data FIS, through a second serial ATA port, from a second host unit;

c. receiving a non-data FIS through a third serial ATA port;

d. arbitrating between the first and second host units and the device;

e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device;

f. coupling the device to the selected one of the first or second host units; [and]

g. while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending non-data FIS to the switch for routing to the device

during the sending step g., the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive;

h. intercepting an original queue depth value from the device, the queue depth value being indicative of the number of commands that the device can queue from either of the first or second host units;

i. altering the original queue depth value to be a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units is the same as the original queue depth value thereby avoiding commands being lost by overrun of the original queue depth value.

Claim 20 (previously amended): A method for communication, as recited in claim 19, further including the steps of transmitting a non-data FIS through the first serial ATA port, non-data FIS through the second serial ATA port, and transmitting a non-data FIS through the third serial ATA port.

Claim 21 (new): A switch, as recited in claim 1, wherein the queue depth value reported to each of the first and second host units is no more than half of the original queue depth value.

Claim 22 (new): A switch, as recited in claim 1, wherein in response to an identify drive command from either of the first or second host units, the arbitration and control circuit is configured to intercept an identify drive response, which is generated by the device in response to the identify drive command, and to replace the original queue depth value with a queue depth value that is no more than one-half that reported by the device.

Claim 23 (new): A switch, as recited in claim 22, wherein the identify drive response includes the identity of the first and second host units.

Claim 24 (new): A switch, as recited in claim 9, wherein the queue depth value reported to each of the first and second host units is no more than half of the original queue depth value.

Claim 25 (new): A switch, as recited in claim 9, wherein in response to an identify drive command from either of the first or second host units, the arbitration and control circuit is configured to intercept an identify drive response, which is generated by the device in response to the identify drive command, and to replace the original queue depth value with a queue depth value that is no more than one-half that reported by the device.

Claim 26 (new): A switch, as recited in claim 25, wherein the identify drive response includes the identity of the first and second host units.

Claim 27 (new): A switch, as recited in claim 14, wherein the queue depth value is no more than one-half of the original queue depth value.

Claim 28 (new): A switch, as recited in claim 14, wherein in response to an identify drive command from either of the first or second host units, the arbitration and control circuit is configured to intercept an identify drive response, which is generated by the device in response to the identify drive command, and to replace the original queue depth value with a queue depth value that is no more than one-half that reported by the device.

Claim 29 (new): A switch, as recited in claim 28, wherein the identify drive response includes the identity of the first and second host units.